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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,014	04/03/2001	Chun-Chi Wang	4006-118	6473

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EXAMINER	
FOONG, SUK SAN	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,014	WANG ET AL.	
	Examiner	Art Unit	
	Suk-San Foong	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6, 9-14 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-14 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The finality of the Office Action mailed 1/8/03 is withdrawn in view of the new grounds of rejection below.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 4 recites the limitation "the step of defining the shallow trench" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 4 recites the limitation "the step of defining the shallow trench" in lines 1-2. There is insufficient antecedent basis for this limitatiòn in the claim.

Claim Rejections - 35 USC § 103

6. Claims 1-4, 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walsh et al. ('741) in combination with Andrews et al. ('709), Sakai et al. ('263) and Lee ('355).

Walsh et al. teaches a method of forming shallow trench isolations which includes providing substrate 10 (Col. 2, lines 39-40), depositing first silicon nitride layer 20 (Col. 2. line 40), then etching silicon nitride layer 20 and substrate 10 to form trenches 25 (Col. 2, line 43), subsequently depositing oxide layer 40 by high density plasma-chemical vapor deposition (HDP-CVD) to fill trenches 25 and over substrate 10 (Col. 2, lines 46-67, Fig. 3), then etching oxide layer 40 to expose edges of first silicon nitride layer 30 (Col. 3 lines 1-4, and Fig. 4), then forming second silicon nitride layer 50 on substrate 10 covering oxide layer 40 and first silicon nitride layer 30 (Col. 3, lines 9-11, and Fig. 5), then forming and patterning photoresist layer 60 over second nitride layer 30 (Col. 3, lines 20-21, and Fig. 6), subsequently etching a portion of second silicon nitride layer 30 (Col. 3, lines 21-22, and Fig. 7), then removing photoresist layer 60 (Fig. 7), then etching oxide layer 40 to expose underling first silicon nitride layer 30 (Col. 3, lines 23-25, and Fig. 8), and removing remaining portions of first silicon nitride layer 30 and second silicon nitride layer 50 (Col. 3, lines 27-29, and Fig. 9).

Walsh et al. does not teach performing a wet etching step to etch the oxide layer until the first silicon nitride layer is about exposed; as recited in claim 1, lines 6-7.

Andrews et al. disclose a method of forming shallow trench isolation which includes providing silicon substrate 10, forming oxide layer 30 on substrate 10, subsequently forming first silicon nitride layer 40 over oxide layer 30 (Paragraph [0017]), then forming shallow trench 20 through first silicon nitride layer 40 and substrate 10 by dry etching (Fig. 1), then forming oxide layer 50 over substrate 10 and filling trench 20 by HDPCVD (Paragraph [0018]), subsequently wet etching oxide layer 50 until first silicon nitride layer 40 is exposed (Paragraph [0021], and Fig. 2), then forming and defining photoresist 60 over trench 20 (Paragraph [0022], and Fig. 3),

subsequently etching a portion of oxide layer 30 by an etching process until first silicon nitride layer is exposed (Fig. 4), then removing photoresist 60 (Paragraph [0023]), then removing remaining portions of oxide layer 50 (Fig. 6), and removing first silicon nitride layer 40 through phosphoric acid wet etching (Paragraph [0023] and Fig. 6).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Walsh et al. with Andrews et al. because it would enable the step of etching oxide layer 40 to expose underling first silicon nitride layer 30 of Walsh et al. to be performed.

The combination process does not disclose etching an exposed portion of the oxide layer.

The combination process does not disclose forming trenches by dry etching; as recited in claim 4.

Sakai et al. discloses a method of forming a shallow trench isolation structure for semiconductor devices which includes providing substrate 1 with first silicon nitride layer 3 formed thereon (Col. 9, lines 36-48, and Fig. 1), then forming trench 21C in substrate 1 by anisotropic etching or dry etching (Col. 9, lines 50-58, and Fig. 2), subsequently forming oxide layer 11 over substrate 1, and, thus in trench 21C by HDP-CVD (Col. 10, lines 24-32, and Fig. 3), subsequently forming photoresist layer 41S over surface of oxide layer 11 (Col. 10, lines 58-60, and Fig. 4), then defining and patterning photoresist layer 41S to form patterned photoresist layer 41, 43 (Col. 10, lines 61-66, and Fig. 5), subsequently etching an exposed portion of oxide layer 11 by dry etching (Col. 11, lines 25-28, and Fig. 6), then removing patterned photoresist layer 41, 43 (Col. 11, lines 55-58), subsequently removing remaining portions of oxide layer 11 on first silicon nitride layer 3 by chemical mechanical polishing (CMP) method (Col. 11, lines

60-63, and Fig. 8), and followed by removal of first nitride layer 3 by wet etching (Col. 12, lines 15-20, and Fig. 9).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Sakai et al. because it would enable removal of a portion of exposed oxide layer 40 to expose underlying silicon nitride layer of the combination process and obtain further advantage of preventing formation of depressions at the edge portion of the trench type element isolation 11, thereby causing no imperfection in device characteristics (Sakai et al., Col. 12, lines 45-49).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Sakai et al. because it would enable formation of trenches 25 of the combination process to be performed.

The combination process does not teach the step as recited in claim 1, lines 14-16.

Lee teaches a method of forming an isolation region for a semiconductor device which includes providing substrate 10 with first silicon nitride layer 12a, 12b formed thereon and trenches 13a, 13b in substrate 10 (Col. 3, lines 40-51, and Fig. 2A), subsequently forming oxide layer 15 over substrate 10 and in trenches 13a, 13b (Col. 3, line 63 to Col. 4, line 34, Fig. 2D), then wet etching oxide layer 15 to expose a portion of first silicon nitride layer 12a, 12b (Col. 4, lines 35-39, and Fig. 2E), and subsequently removing oxide layer 15 while removing first silicon nitride layer 12a, 12b by hot phosphoric acid (H_3PO_4) (Col. 4, lines 58-61, and Fig. 2F).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Lee because it would enable the step of removing

remaining portions of first silicon nitride layer 30 and second silicon nitride layer 50 and thus removal the remaining portion of oxide layer 40 of the combination process to be performed.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walsh et al. ('741) in combination with Andrews et al. ('709), Sakai et al. ('263) and Lee ('355) as applied to claims 1-4, 6 and 17 above, and further in view of Wolf.

The combination process does not disclose etching second silicon nitride layer by dry etching.

Wolf teaches etching of silicon nitride layers by a dry etching process (pgs. 555-556).

It would have been within the scope to one ordinary skill in the art to combine the teachings of the combination process with Wolf because it would enable the step of etching a portion second silicon nitride layer 50 of combination process to be performed.

8. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. ('263) in combination with Lee ('355).

Sakai et al. discloses a method of forming a shallow trench isolation structure for semiconductor devices which includes providing substrate 1 with first silicon nitride layer 3 formed thereon (Col. 9, lines 36-48, and Fig. 1), then forming trench 21C in substrate 1 by anisotropic etching or dry etching (Col. 9, lines 50-58, and Fig. 2), subsequently forming oxide layer 11 over substrate 1, and, thus in trench 21C by HDP-CVD (Col. 10, lines 24-32, and Fig. 3), subsequently forming photoresist layer 41S over surface of oxide layer 11 (Col. 10, lines 58-60, and Fig. 4), then defining and patterning photoresist layer 41S to form patterned photoresist

layer 41, 43 (Col. 10, lines 61-66, and Fig. 5), subsequently etching an exposed portion of oxide layer 11 by dry etching (Col. 11, lines 25-28, and Fig. 6), then removing patterned photoresist layer 41, 43 (Col. 11, lines 55-58), subsequently removing remaining portions of oxide layer 11 on first silicon nitride layer 3 by chemical mechanical polishing (CMP) method (Col. 11, lines 60-63, and Fig. 8), and then removing of first nitride layer 3 by wet etching (Col. 12, lines 15-20, and Fig. 9).

Sakai et al. does not teach performing a wet etching step to etch the oxide layer until the first silicon nitride layer is about exposed; as recited in claim 9, lines 6-7.

Sakai et al. does not teach the step as recited in claim 9, lines 12-13.

Lee teaches a method of forming an isolation region for a semiconductor device which includes providing substrate 10 with first silicon nitride layer 12a, 12b formed thereon and trenches 13a, 13b in substrate 10 (Col. 3, lines 40-51, and Fig. 2A), subsequently forming oxide layer 15 over substrate 10 and in trenches 13a, 13b (Col. 3, line 63 to Col. 4, line 34, Fig. 2D), then wet etching oxide layer 15 to expose a portion of first silicon nitride layer 12a, 12b (Col. 4, lines 35-39, and Fig. 2E), and subsequently removing oxide layer 15 while removing first silicon nitride layer 12a, 12b by wet etching such as hot phosphoric acid (H_3PO_4) (Col. 4, lines 58-61, and Fig. 2F).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Sakai et al. with Lee because it would enable the steps of removing remaining portions of first silicon nitride layer 3, and, thus remaining portion of oxide layer 11 of Sakai et al. to be performed.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 9 and 17, and claims dependent thereon have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Son et al. ('056) uses a lift-off process to remove remaining portions of oxide layer formed of silicon nitride layer instead of CMP process in order to reduce contamination of semiconductor substrate and enchance the productivity in a semiconductor fabrication process. Kim et al. ('696) discloses an etching of insulating layer for trench-filing, then etching the insulating layer to expose an underlying nitride layer and subsequently performing a wet etching process with respect to the nitride layer thereby lifting-off the insulating layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

April 28, 2003

George Fourson
Primary Examiner
Art Unit 2823